REMARKS

This paper responds to the Office Action mailed on July 21, 2005.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

Examiner's 892 Form

Applicant notes that in the Office Action dated July 21, 2005, the Examiner has relied upon EP patent 0678904A1 to Boruta. However, this patent is not listed on the Examiner's 892 Form, and has not previously been cited in the application. Applicant respectfully requests that the Examiner list the Boruta reference on an 892 Form with the next Office Action, so that this documents is listed as being of record in this application.

Objections to the Claims

Claims 17 and 39 were objected to under 37 CFR 1.75 (c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant has amended the base claims herein, so that claims 17 and 39 now further limit the base claims and respectfully submits that the claims are now in conformance with 37 CFR 1.75 (c). In view of the noted amendments, Applicant respectfully requests that this objection be withdrawn.

§112 Rejection of the Claims

Claims 11-25, 35-39, and 41-43 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the term "polished" is stated to be indefinite.

Applicant respectfully submits that the Office Action is incorrect in stating on page 2 that "the specification does not provide a standard for ascertaining the requisite degree" of polishing. Applicant respectfully submits that one of ordinary skill in the art would understand the "invention involves further removing the layer of remaining scribe 22 on the die and also increasing the smoothness and flatness of the perimeter edges 18 ... each die is further ground or polished ...to remove a substantial amount of the remaining scribe 22 and reduce or eliminate

any irregularities 24 in the edges 18", as discussed in the specification at least at page 7. Applicant respectfully submits that one of ordinary skill in the art would understand that a "circuit die may be held by a carrier and forced against a rotary grinding disc or polishing pad", where "the pad or disc is typically impregnated with a chemical or abrasive slurry which contacts the die edge to remove a portion of the scribe from the edges 18 and the pad or disc rotates", as discussed in the specification at least at page 8.

Applicant submits that the term "polished" is definite and understood by one of ordinary skill in the art, and that the requisite degree of polishing is clear as being enough to remove the irregularities caused by sawing the die from the wafer, as noted in the above portions of the specification.

Applicant further respectfully submits that the amendments contained herein to independent claims 11, 15, 18, 22, 25, 35 and 41, further clarify the limits of the claims and place the rejected claims in patentable condition. The dependent claims are felt to be patentable at least as depending from base claims shown above to be patentable. In view of the above noted amendments to the independent claims Applicant respectfully requests that this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 11-16, 18-25, 35-38, and 41-43 were rejected under 35 USC § 103(a) as being unpatentable over Boruta (EP 06478904A1) in view of Altavela (U.S. Patent No. 5,408,739) and Arit et al. (U.S. Patent No. 4,804,641). Applicant respectfully traverses this rejection.

The cited reference of Boruta discloses a method of sawing or cutting a wafer that has metal material in the scribe lines, where the metal material is wider than the saw blade. The method includes making three saw cuts, the first two cuts being partial cuts not going through the thickness of the wafer and separated by less than the thickness of the saw blade (see Figs. 2A, 2B, 2C and 2D; and col. 1, lines 26-33).

The cited reference of Altavela discloses a two step method of sawing a front surface of a thermal ink jet printer head so that the sawing leaves a front surface that does not require a polishing step (see Fig. 8 and col. 1, lines 7-14).

The cited reference of Arit discloses an additional ring of specially grown thermal oxide that surrounds the active area of a chip to act as a crack stopper and prevent the wafer sawing from producing chips that penetrate the active area.

The cited Arit reference is used in the outstanding Office Action to show that it is known in the art that wafer sawing creates cracks. Applicant agrees with the Examiner that cracks caused by wafer sawing (as shown by the Arit reference) are a known problem in the art, as is stated in the present specification at least at page 3, lines 2-3 where it states that the "method further produces a die which is less susceptible to damage such as edge chip or die cracking". Applicant notes that the solution envisioned by Arit to the known edge chip problem includes increasing the size of the die by at least the width of the separately grown oxide ring (greater than 5 microns) plus a safety region of greater than 5 microns (see figure 2 and col.3, lines 13-29), which ignoring the unspecified spacing between the oxide 1 and the scribe line 8, adds more than 20 microns to both the length and the width of the IC die. This is in direct opposition to the present invention which teaches among other things an "integrated circuit die which is slightly smaller in length and width than a conventionally produced die", and that a "size reduction of nearly 100 μm in length and width may be quite significant in some applications" (see page 3, lines 1-2 and page 7, lines 11-12). Applicant respectfully submits that one of ordinary skill in the art would not be motivated to combine a reference such as Arit that results in an additional process step and an additional 20 microns of die size and width, with the other suggested combinations of references, to obtain an invention that reduces the die size in addition to resolving the chip problem. Applicant submits that the suggested combination is improper as lacking motivation to combine.

Applicant respectfully submits that the suggested Altavela reference and its disclosed sawn ***front face*** surface would not provide motivation for one of ordinary skill in the art to combine its teaching with the other suggested references to obtain the present invention using grinding and polishing to remove irregularities and to reduce the size of the IC die. Since there is no suggestion in the cited reference of reducing the size of the die or of removing irregularities, the suggested combination is improper as lacking motivation to combine.

Applicant respectfully submits that the Boruta reference does not disclose or suggest an unused buffer region around active circuitry wherein the region is within 5 microns of the active

edge. Applicant notes that this omission is properly noted in the outstanding Office Action in the second paragraph on page 4. Applicant submits that the Examiner is incorrect to state that Arit suggests a scribe edge within 5 microns of the active area. As discussed above, the Arit reference teaches adding an additional 5 microns of "safety space" plus an additional 5 microns of an oxide ring around the active region before getting to the unspecified space between the oxide ring 1 and the scribe 8. Therefore, the scribe edge of Arit could not possibly be within 5 microns of the active area edge. Thus, the suggested combination of references, even if there were proper motivation to make the combination, still does not result in the claimed arrangement.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the combination of features of "*...each planar perimeter side surface of the semiconductor die being a surface substantially perpendicular to the first planar surface, having a lateral portion of the second region removed by a smoothing material removal process from the lateral direction with a top portion of each individual planar perimeter side surface disposed in the second region and within approximately 5 microns of an edge of the first region....*", as recited in independent claim 11, as amended herein. For essentially similar reasons the other independent claims are believed to be patentable as amended herein over the suggested combination of references. None of the suggested references contain this feature.

The independent claims have been shown above to be patentable over the suggested combination of references. The dependent claims are believed to be in patentable condition at least as depending upon base claims shown above to be patentable over the suggested combination of references.

In view of the above discussed amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorneys, Tim Clise at (612) 349-9587 or David Suhl at (508) 865-8211 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 12 Oct '05 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13 day of October, 2005.

KACIA LEE _____
Name

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Signature